

Employee Locator

query by organization

14 Records Were Found

Employee	Office	Building	Fl.-Ste./Corr.- Rm	Contact No.	Type	Ext
→ <u>ANDERSON MATTHEW D</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/B20</u>	<u>(703)306-5931</u>	T	
<u>BATAILLE PIERRE MICHE (PIERRE-MICHE)</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/D08</u>	<u>(703)305-0134</u>	T	
<u>CHOI WOO H</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/A22</u>	<u>(703)305-3845</u>	T	
<u>ELMORE STEPHEN C</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/C19</u>	<u>(703)308-6256</u>	T	
<u>KIM HONG C</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/D10</u>	<u>(703)305-3835</u>	T	
<u>KIM MATTHEW (MATT) M (SPE)</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/R01</u>	<u>(703)305-3821</u>	T	
<u>LI ZHUO H</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/A10</u>	<u>(703)305-3846</u>	T	
<u>PATEL HETUL B</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/A33</u>	<u>(703)305-6219</u>	T	
<u>PEIKARI BEHZAD</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/Y11</u>	<u>(703)305-3824</u>	T	
<u>ROBERTSON DAVID (DAVID L.) L</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/Y09</u>	<u>(703)305-3825</u>	T	
<u>SHAH SAUMIL R</u>	<u>P/2186</u>	<u>PK2</u>	<u>03/C22</u>	<u>(703)305-8786</u>	T	
<u>THAI TUAN V</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/R11</u>	<u>(703)305-3842</u>	T	
<u>THOMAS SHANE M</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/A08</u>	<u>(703)605-0725</u>	T	
<u>TRAN DENISE</u>	<u>P/2186</u>	<u>PK2</u>	<u>02/R03</u>	<u>(703)305-9823</u>	T	

Contact Number Type: T - Telephone, F - Fax, R - Receptionist, P - Pager, M - Mobile

REG BRAG DON

Employee Search Completed
No more records to search

⊗ Memory Accessing, Addressing.



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Class 711 ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY

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1 ADDRESSING COMBINED WITH SPECIFIC MEMORY CONFIGURATION OR SYSTEM

- 2 . Addressing extended or expanded memory
- 3 . Addressing cache memories
- 4 . Dynamic-type storage device (e.g., disk, tape, drum)
- 5 . For multiple memory modules (e.g., banks, interleaved memory)
- 6 . Virtual machine memory addressing

100 STORAGE ACCESSING AND CONTROL

- 101 . Specific memory composition
- 102 .. Solid-state read only memory (ROM)
- 103 ... Programmable read only memory (PROM, EEPROM, etc.)
- 104 .. Solid-state random access memory (RAM)
- 105 ... Dynamic random access memory
- 106 Refresh scheduling
- 107 .. Ferrite core
- 108 .. Content addressable memory (CAM)
- 109 .. Shift register memory
- 110 ... Circulating memory
- 111 .. Accessing dynamic storage device
- 112 ... Direct access storage device (DASD)
- 113 Caching
- 114 Arrayed (e.g., RAID's)
- 115 .. Detachable memory
- 116 .. Bubble memory
- 117 . Hierarchical memories
- 118 .. Caching
- 119 ... Multiple caches
- 120 Parallel caches
- 121 Private caches
- 122 Hierarchical caches
- 123 User data cache and instruction data cache
- 124 Cross-interrogating
- 125 ... Instruction data cache
- 126 ... User data cache
- 127 ... Interleaved
- 128 ... Associative
- 129 ... Partitioned cache

<u>130</u>	... Shared cache
<u>131</u>	... Multiport cache
<u>132</u>	... Stack cache
<u>133</u>	... Entry replacement strategy
<u>134</u> Combined replacement modes
<u>135</u> Cache flushing
<u>136</u> Least recently used
<u>137</u>	... Look-ahead
<u>138</u>	... Cache bypassing
<u>139</u> No-cache flags
<u>140</u>	... Cache pipelining
<u>141</u>	... Coherency
<u>142</u> Write-through
<u>143</u> Write-back
<u>144</u> Cache status data bit
<u>145</u> Access control bit
<u>146</u> Snooping
<u>147</u>	. Shared memory area
<u>148</u>	.. Plural shared memories
<u>149</u>	.. Multiport memory
<u>150</u>	.. Simultaneous access regulation
<u>151</u>	.. Prioritized access regulation
<u>152</u>	.. Memory access blocking
<u>153</u>	.. Shared memory partitioning
<u>154</u>	. Control technique
<u>155</u>	.. Read-modify-write (RMW)
<u>156</u>	.. Status storage
<u>157</u>	.. Interleaving
<u>158</u>	.. Prioritizing
<u>159</u>	.. Entry replacement strategy
<u>160</u>	... Least recently used (LRU)
<u>161</u>	.. Archiving
<u>162</u>	... Backup
<u>163</u>	.. Access limiting
<u>164</u>	... With password or key
<u>165</u>	.. Internal relocation
<u>166</u>	.. Resetting
<u>167</u>	. Access timing
<u>168</u>	.. Concurrent accessing
<u>169</u>	.. Memory access pipelining
<u>170</u>	. Memory configuring
<u>171</u>	.. Based on data size
<u>172</u>	.. Based on component size
<u>173</u>	.. Memory partitioning
<u>200</u>	ADDRESS FORMATION
<u>201</u>	. Slip control, misaligning, boundary alignment
<u>202</u>	. Address mapping (e.g., conversion, translation)



- 203 .. Virtual addressing
- 204 ... Predicting, look-ahead
- 205 Directories and tables (e.g., DLAT, TLB)
- 206 ... Translation tables (e.g., segment and page table or map)
- 207 Directory tables (e.g., DLAT, TLB)
- 208 Segment or page table descriptor
- 209 ... Including plural logical address spaces, pages, segments, blocks
- 210 .. Resolving conflict, coherency, or synonym problem
- 211 . Address multiplexing or address bus manipulation
- 212 . Varying address bit-length or size
- 213 . Generating prefetch, look-ahead, jump, or predictive address
- 214 . Operand address generation
- 215 . In response to microinstruction
- 216 . Hashing
- 217 . Generating a particular pattern/sequence of addresses
- 218 .. Sequential addresses generation
- 219 . Incrementing, decrementing, or shifting circuitry
- 220 . Combining two or more values to create address
- 221 . Using table

FOREIGN ART COLLECTIONS

FOR000 **CLASS-RELATED FOREIGN DOCUMENTS**

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